What is claimed is:

1. A method for generating a refresh clock of a DRAM module, wherein the DRAM module comprises a plurality of memory cells, each of the memory cells having a storage capacitor, comprising:

providing a dummy capacitor, the dummy capacitor has a positive correlation with the storage capacitor; and

generating a refresh clock according to a capacitance of the dummy capacitor;

wherein a refresh interval of the refresh clock is positively correlated with the capacitance of the dummy capacitor.

2. The method for generating a refresh clock of claim 1, further comprising a method for generating the refresh clock:

providing an oscillator for generating the refresh clock, wherein the dummy capacitor is an oscillator load.

3. The method for generating a refresh clock of claim 1, wherein the dummy capacitor is one of the storage capacitors.

4. A refresh clock generator of a DRAM module, wherein the DRAM module comprises a plurality of memory cells, each of the memory cells having a storage capacitor, comprising:

a dummy capacitor positively correlated with the storage capacitor; and

a clock generator for generating a refresh clock, and coupling to the dummy capacitor;

wherein a refresh interval of the refresh clock is positively correlated with a capacitance of the dummy capacitor.

5. The refresh clock generator of claim 4, wherein the clock generator is a ring oscillator and the dummy capacitor is a ring oscillator load.

6. The refresh clock generator of claim 5, wherein the refresh clock generator comprises a plurality of dummy capacitors, the ring oscillator comprises a plurality of inverters, and each output terminal of the inverters couples to a corresponding dummy capacitor.

7. The refresh clock generator of claim 4, wherein the dummy capacitor is one of the storage capacitors.